REMARKS

The following remarks are submitted as a full and complete response to the outstanding Action. By this Amendment, claims 1, 4, 7 and 12 have been amended, and new claims 19 to 26 have been added to further set forth the instant application. No new matter has been introduced. Currently, claims 1-17 and 19-26 are pending and therefore submitted for consideration.

Title

The title has been objected to as being non- descriptive.

In response, the title has been amended to overcome the objection.

Claim Rejection

Claims 1-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Maruyama et al.* (US Patent Pub. No. 2001/0003199, hereinafter "*Maruyama*") in view of *Dye* (U.S. Patent No. 6,173,381) and *Lopez-Auado* (U.S. Patent No. 5,586,283).

The Examiner has purported that the combination of the cited references of ***Maruyama, Dye*** and ***Lopez-Auado*** would render the present application as set forth in claims 1-17 obvious. However, for at least the reasons stated below, it is respectfully submitted that such hindsight combination is not proper because, e.g., there are no motivations or suggestions found in the cited references for such combination.

Maruyama discloses that an address conversion destination of a program space can be switched to be set between a first memory ROM and a second memory RAM, using a single decoder 16.

Dye discloses two address conversion units 140a and 140b (see Fig. 3B) for controlling a plurality of memory units. It is noted that these address conversion units are not equivalent to the first address conversion unit and the second address conversion unit as recited in independent claims 1, 4, 7, and 12 of the present application.

Lopez-Aguado also discloses one address conversion unit including a comparator that compares a requested logical address with logical addresses to which physical addresses of memory units have been assigned.

Accordingly, none of ***Dye***, ***Maruyama***, and ***Lopez-Aguado*** discloses or teaches the present application as now set forth in claims 1-17 that requires a first address conversion unit which carries out a first address conversion by assigning a first physical address of a first memory unit to a first logical address of a load module stored in the first memory unit, the load module including an instruction code and numerical data, and a second address conversion unit which carries out a second address conversion different from the first address conversion by assigning a second physical address of a second memory unit to a second logical address of the instruction code that has been copied to the second memory unit.

Accordingly, Applicant requests the withdrawal of the rejection of claims 1-17 under 35 U.S.C. 103(a).

In view of the foregoing, allowance of claims 1-17 and 19-26 and the prompt issuance of a Notice of Allowability are respectfully solicited.

In the event this paper is not considered to be timely filed, Applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300.

The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300.

Respectfully submitted,

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